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## IN THE CLAIMS:

1. (currently amended) A system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising:

a baseband processor that is operable to receive analog signals corresponding to a data block  
5 and to sample the analog signal to produce samples corresponding to the data block;

an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block, the baseband processor and equalizer together operable to perform a substantial portion of Physical (PHY) layer operations of the system;

10 a system processor that is operable to execute a substantial portion of Media Access Control (MAC) layer operations of the system, to receive the soft decision bits of the data block from the equalizer, to, prior to executing all MAC layer operations on the soft decision bits, investigate whether IR operations are required for the soft decision bits of the data block, and to initiate IR operations based upon the investigation; and

15 an IR processing module operably coupled to the system processor that is operable to receive the soft decision bits of the data block, to receive a direction from the system processor to perform IR operations on the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block.

20 2. (currently amended) The system of claim 1, wherein the system processor is operable to decode the soft decision bits to produce a decoded header for the data block and to determine whether IR operations are required for the soft decision bits of the data block based upon the decoded header.

3. (currently amended) The system of claim 1, wherein the system processor is operable to implement at least one process that logically separates the PHY layer operations of the baseband processor from its MAC layer operations, the at least one process operable to:

5 determine that IR operations are required for the soft decision bits of the data block; and  
to initiate the IR operations of the IR processing module, the IR processing module is  
operable to decode the soft decision bits to produce a decoded header for the data block.

4. (original) The system of claim 1, wherein in performing IR operations:  
10 a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block  
is determined;

the soft decision bits are deinterleaved;

the soft decision bits are depunctured to produce depunctured soft decision bits; and

the IR processing module is operable to decode the depunctured soft decision bits.

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5. (original) The system of claim 1, wherein when the IR operations are  
unsuccessful, the soft decision bits of the data block are stored in IR memory.

6. (original) The system of claim 5, wherein during IR operations on a subsequently  
20 received copy of the data block:

a determination is made that a Modulation and Coding Scheme (MCS) mode and  
puncturing pattern of the subsequently received copy of the data block and a MCS mode of the  
data block are compatible;

soft decision bits of the subsequently received copy of the data block are combined with soft decision bits of the data block to produce combined soft decision bits;

the combined soft decision bits are depunctured; and

the IR processing module decodes the depunctured combined soft decision bits.

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7. (original) The system of claim 5, wherein during IR operations on a subsequently received copy of the data block:

a determination is made that a Modulation and Coding Scheme (MCS) mode of the subsequently received copy of the data block and a MCS mode and puncturing pattern of the data

10 block are compatible;

the soft decision bits of the data block are depunctured to produce first depunctured soft decision bits;

the soft decision bits of data of the subsequently received copy of the data block are depunctured to produce second depunctured soft decision bits;

15 the first depunctured soft decision bits and the second depunctured soft decision bits are combined to produce combined depunctured soft decision bits; and

the IR processing module is operable to decode the combined depunctured soft decision bits.

20 8. (original) The system of claim 1, wherein the IR processing module operates as a slave to the system processor.

9. (original) The system of claim 1, wherein:

the system processor interfaces with the IR processing module via a plurality of registers;  
and  
the IR processing module asserts an interrupt to the system processor to indicate the completion of a processing task.

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10. (original) The system of claim 1, wherein the system supports Modulation and Coding Scheme (MCS) modes of the GSM EDGE standardized protocol.

11. (original) The system of claim 1, further comprising IR memory including Type I  
10 IR memory and Type II IR memory, wherein control information is stored in Type I IR memory and soft decision bits are stored in Type II IR memory.

12. (original) The system of claim 11, wherein either punctured soft decision bits or depunctured soft decision bits may be stored in each Type II IR memory location.

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13. (original) The system of claim 1, wherein the data block may include a complete Radio Link Control (RLC) block or a segmented RLC block.

14. (currently amended) A system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising:

at least one processing device that is operable to execute a substantial portion of Physical (PHY) layer operations and a substantial portion of Media Access Control (MAC) layer operations

5 of the system, the at least one processing device:

performing the PHY layer operations to receive an analog signal corresponding to a data block, to sample the analog signal to produce samples, to equalize the samples, and to produce soft decision bits of the data block; and

intervening between the PHY layer operations and the MAC layer operations to  
10 determine that IR operations are required for the soft decision bits of the data block, and to initiate IR operations; and

an IR processing module operably coupled to the at least one processing device that is operable to receive the soft decision bits of the data block, to receive a direction from the at least one processing module to perform IR operations on the soft decision bits of the data block, and to  
15 perform IR operations on the soft decision bits of the data block.

15. (currently amended) The system of claim 14, wherein the at least one processing device is operable to decode the soft decision bits to produce a decoded header for the data block and to determine whether IR operations are required for the soft decision bits of the data block  
20 based upon the decoded header.

16. (currently amended) The system of claim 14, wherein the at least one processing module is operable to implement at least one process that logically separates the PHY layer

operations from the MAC layer operations, the at least one process operable to:

determine that IR operations are required for the soft decision bits of the data block; and

to initiate the IR operations of the IR processing module, the IR processing module is  
operable to ~~decode the soft decision bits to produce a decoded header for the data block.~~

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17. (original) The system of claim 14, wherein in performing IR operations:

a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block  
is determined;

the soft decision bits are depunctured to produce depunctured soft decision bits; and

10 the IR processing module is operable to decode the depunctured soft decision bits.

18. (original) The system of claim 14, wherein when the IR operations are  
unsuccessful, the soft decision bits of the data block are stored in IR memory.

15 19. (original) The system of claim 18, wherein during IR operations on a  
subsequently received copy of the data block:

a determination is made that a Modulation and Coding Scheme (MCS) mode and  
puncturing pattern of the subsequently received copy of the data block and a MCS mode and  
puncturing pattern of the data block are compatible;

20 soft decision bits of the subsequently received copy of the data block are combined with  
soft decision bits of the data block to produce combined soft decision bits;

the combined soft decision bits are depunctured; and

the IR processing module decodes the depunctured combined soft decision bits.

20. (original) The system of claim 18, wherein during IR operations on a subsequently received copy of the data block:

a determination is made that a Modulation and Coding Scheme (MCS) mode of the subsequently received copy of the data block and a MCS mode of the data block are compatible;

the soft decision bits of the data block are depunctured to produce first depunctured soft decision bits;

the soft decision bits of data of the subsequently received copy of the data block are depunctured to produce second depunctured soft decision bits;

the first depunctured soft decision bits and the second depunctured soft decision bits are combined to produce combined depunctured soft decision bits; and

the IR processing module is operable to decode the combined depunctured soft decision bits.

21. (original) The system of claim 14, wherein the IR processing module operates as a slave to the at least one processing device.

22. (original) The system of claim 14, wherein:

the at least one processing device interfaces with the IR processing module via a plurality of registers; and

the IR processing module asserts an interrupt to the at least one processing device to indicate the completion of a processing task.

23. (original) The system of claim 14, wherein the system supports Modulation and Coding Scheme (MCS) modes of the GSM EDGE standardized protocol.

24. (original) The system of claim 14, further comprising IR memory including Type  
5 I IR memory and Type II IR memory, wherein control information is stored in Type I IR memory and soft decision bits are stored in Type II IR memory.

25. (original) The system of claim 24, wherein either punctured soft decision bits or depunctured soft decision bits may be stored in each Type II IR memory location.

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26. (original) The system of claim 14, wherein the data block may include a complete Radio Link Control (RLC) block or a segmented RLC block.

27. (currently amended) A method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising:

by at least one processing device that is operable to execute a substantial portion of Physical (PHY) layer operations and a substantial portion of Media Access Control (MAC) layer operations

5 of the wireless receiver:

performing PHY layer operations including:

receiving an analog signal corresponding to a data block;

sampling the analog signal to produce samples; and

equalizing the samples to produce soft decision bits of the data block;

10 intervening between the PHY layer operations and the MAC layer operations to determine that IR operations are required for the soft decision bits of the data block; and

transferring the soft decisions of the data block to an IR processing module along with a direction to perform IR operations on the soft decisions of the data block; and

the IR processing module receiving the soft decision bits of the data block and performing  
15 IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

28. (original) The method of claim 27, wherein the IR operations include:

decoding the soft decision bits of the data block to produce a decoded header; and

20 determining a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header;

depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and

the IR processing module decoding the depunctured soft decision bits.

29. (original) The method of claim 28, wherein the IR processing module performs the depuncturing operations.

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30. (original) The method of claim 27, further comprising:  
failing to correctly decode the soft decision bits of the data block;  
storing the soft decision bits of the data block in an IR memory;  
receiving a new copy of the data block;

10 determining that a Modulation and Coding Scheme (MCS) mode of the data block and a MCS mode of the new copy of the data block are compatible;

combining soft decision bits of the new copy of the data block with soft decision bits of the data block to produce combined soft decision bits; and

the IR processing module decoding the combined soft decision bits.

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31. (original) The method of claim 30, further comprising:  
failing to correctly decode the combined soft decision bits; and  
storing the combined soft decision bits in an IR memory.

20 32. (original) The method of claim 30, wherein combining soft decision bits of the new copy of the data block with soft decision bits of the data block to produce combined soft decision bits comprises combining punctured soft decision bits when:

a MCS mode of the data block is the same as a MCS mode of the new copy of the data block; and

a puncturing pattern of the data block is the same as a puncturing pattern of the new copy of the data block.

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33. (original) The method of claim 30, wherein combining soft decision bits of the new copy of the data block with soft decision bits of the data block to produce combined soft decision bits comprises:

depuncturing the soft decision bits of the data block to produce first depunctured soft decision bits;

depuncturing the soft decision bits of the new copy of the data block to produce second depunctured soft decision bits; and

combining the first depunctured soft decision bits with the second depunctured soft decision bits to produce the combined soft decision bits.

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34. (original) The method of claim 27, wherein:

each symbol of the data block is represented by four punctured soft decision bits; and

each symbol of the data block is also represented by five depunctured soft decision bits.